WHAT IS CLAIMED IS:

1. A process for producing a display comprising the steps of:

forming a crystalline semiconductor film by a process comprising:

a semiconductor film deposition process in which a semiconductor film is deposited on a substrate,

a first annealing process in which said semiconductor film is crystallized by repeatedly performing a process that melt crystallizes a portion of said semiconductor film, and

a second annealing process in which rapid thermal annealing is performed on said crystallized semiconductor film,

wherein an annealing temperature in the second annealing process is expressed by the absolute temperature T and, when the annealing time is t, expressed in seconds, annealing temperature T and annealing time t satisfy the relationship:

$$1.72 \times 10^{-21}\ \text{sec} < t \cdot \exp(-\varepsilon/kT) < 4.63 \times 10^{-14}\ \text{sec}$$

wherein $\varepsilon = 3.01$ eV and $k = 8.617 \times 10^{-5}$ eV/K; and

forming a panel equipped with a device using the semiconductor film.

2. A process for producing a display according to claim 1, wherein an annealing temperature in the second annealing process is expressed by the absolute temperature T and, when the annealing time is t, expressed in seconds, annealing temperature T and annealing time t satisfy the relationship:

$$5 \times 10^{-18}\ \text{sec} < t \cdot \exp(-\varepsilon/kT) < 4.63 \times 10^{-14}\ \text{sec}$$

wherein $\varepsilon = 3.01$ eV and $k = 8.617 \times 10^{-5}$ eV/K.

3. A process for producing a display according to claim 1, wherein an annealing temperature in the second annealing process is expressed by the absolute temperature T and, when the annealing time is t, expressed in seconds, annealing temperature T and annealing time t satisfy the relationship:

$$1.72 \times 10^{-21}\ \text{sec} < t \cdot \exp(-\varepsilon/kT) < 1.09 \times 10^{-15}\ \text{sec}$$

wherein $\varepsilon = 3.01$ eV and $k = 8.617 \times 10^{-5}$ eV/K.

4. A process for producing a display according to claim 1, wherein an annealing temperature in the second annealing process is expressed by the absolute temperature T and, when the annealing time is t, expressed in seconds, annealing temperature T and annealing time t satisfy the relationship:

5×10^{-18} sec $< t \cdot \exp(-\varepsilon/kT) < 1.09 \times 10^{-15}$ sec

wherein $\varepsilon = 3.01$ eV and $k = 8.617 \times 10^{-5}$ eV/K.

5. A process for producing a display according to claim 3, wherein said substrate is glass and said annealing temperature T is below a strain point of said glass substrate.

6. A process for producing a display according to claim 1, wherein said annealing time t is 300 seconds.

7. A process for producing a display according to claim 1, wherein said annealing time t is 180 seconds or less.

8. A process for producing an electronic device comprising the steps of:

forming a crystalline semiconductor film by a process comprising:

a semiconductor film deposition process in which a semiconductor film is deposited on a substrate,

a first annealing process in which said semiconductor film is crystallized by repeatedly performing a process that melt crystallizes a portion of said semiconductor film, and

a second annealing process in which rapid thermal annealing is performed on said crystallized semiconductor film,

wherein an annealing temperature in the second annealing process is expressed by the absolute temperature T and, when the annealing time is t, expressed in seconds, annealing temperature T and annealing time t satisfy the relationship:

1.72×10^{-21} sec $< t \cdot \exp(-\varepsilon/kT) < 4.63 \times 10^{-14}$ sec

wherein $\varepsilon = 3.01$ eV and $k = 8.617 \times 10^{-5}$ eV/K;

forming a panel equipped with a device using the semiconductor film; and

installing the panel in a body of an electronic device.

9. A process for producing an electronic device according to claim 8, wherein an annealing temperature in the second annealing process is expressed by the absolute temperature T and, when the annealing time is t, expressed in seconds, annealing temperature T and annealing time t satisfy the relationship:

5×10^{-18} sec $< t \cdot \exp(-\varepsilon/kT) < 4.63 \times 10^{-14}$ sec

wherein $\varepsilon = 3.01$ eV and $k = 8.617 \times 10^{-5}$ eV/K.

10. A process for producing an electronic device according to claim 8, wherein an annealing temperature in the second annealing process is expressed by the absolute temperature T and, when the annealing time is t, expressed in seconds, annealing temperature T and annealing time t satisfy the relationship:

$$1.72 \times 10^{-21} \text{ sec} < t \cdot \exp(-\varepsilon/kT) < 1.09 \times 10^{-15} \text{ sec}$$

wherein $\varepsilon = 3.01$ eV and $k = 8.617 \times 10^{-5}$ eV/K.

11. A process for producing an electronic device according to claim 8, wherein an annealing temperature in the second annealing process is expressed by the absolute temperature T and, when the annealing time is t, expressed in seconds, annealing temperature T and annealing time t satisfy the relationship:

$$5 \times 10^{-18} \text{ sec} < t \cdot \exp(-\varepsilon/kT) < 1.09 \times 10^{-15} \text{ sec}$$

wherein $\varepsilon = 3.01$ eV and $k = 8.617 \times 10^{-5}$ eV/K.

12. A process for producing an electronic device according to claim 10, wherein said substrate is glass and said annealing temperature T is below a strain point of said glass substrate.

13. A process for producing an electronic device according to claim 8, wherein said annealing time t is 300 seconds.

14. A process for producing an electronic device according to claim 8, wherein said annealing time t is 180 seconds or less.